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L27: Entry 8 of 25

File: USPT

May 15, 2001

DOCUMENT-IDENTIFIER: US 6233717 B1

TITLE: Multi-bit memory device having error check and correction circuit and method for checking and correcting data errors therein

Brief Summary Text (25):

These and other objects, advantages and features of the present invention are provided by storing normal data information into a plurality of first memory cells (i.e., multibit memory cells) each storing more than two possible data states, wherein each data state is represented by two or more data bits and the respective data bits are classified into two or more groups (or sets), and by storing two or more groups of parity bits corresponding to the two or more groups of the data bits respectively into a plurality of second memory cells (single bit memory cells or multibit memory cells). The memory devices include a plurality of sense amplifiers for sensing the two or more groups of the data bits and a plurality of data latches for latching the two or more groups of the sensed data bits, respectively. Each of the sense amplifiers corresponds to at least two of the data latches depending upon bits per cell, and the plurality of the data latches are classified into two or more groups each including only one of the at least two data latches corresponding to each sense amplifier. In particular, the memory devices include an ECC circuit which checks error bits out of the latched data bits sequentially by the group and corrects the checked error bits sequentially by the group.

## Refine Search

### Search Results -

Terms	Documents
L16 same L12	3

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
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 EPO Abstracts Database  
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 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L17





### Search History

DATE: Wednesday, January 28, 2004    [Printable Copy](#)    [Create Case](#)

#### Set Name Query

side by side

#### Hit Count Set Name

result set

*DB=USPT; PLUR=YES; OP=OR*

<u>L17</u>	L16 same l12	3	<u>L17</u>
<u>L16</u>	correct\$ near4 writing	2322	<u>L16</u>
<u>L15</u>	L14 same l9	28	<u>L15</u>
<u>L14</u>	correct\$ same writing	10461	<u>L14</u>
<u>L13</u>	L12 and l11	24	<u>L13</u>
<u>L12</u>	l9 same writ\$	120	<u>L12</u>
<u>L11</u>	L9 same test\$	35	<u>L11</u>
<u>L10</u>	L9 same bisr	0	<u>L10</u>
<u>L9</u>	L8 same memory same cell	289	<u>L9</u>
<u>L8</u>	ecc same correct\$	5253	<u>L8</u>
<u>L7</u>	L6 same cell	18	<u>L7</u>
<u>L6</u>	L5 same memory	27	<u>L6</u>
<u>L5</u>	L4 same l3	30	<u>L5</u>
<u>L4</u>	error	376725	<u>L4</u>

<u>L3</u>	bisr	72	<u>L3</u>
<u>L2</u>	L1 same memory	40	<u>L2</u>
<u>L1</u>	ecc same repair	66	<u>L1</u>

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L24: Entry 7 of 24

File: USPT

May 2, 2000

DOCUMENT-IDENTIFIER: US 6058047 A

TITLE: Semiconductor memory device having error detection and correction

## CLAIMS:

12. A method of writing/reading data with regard to a semiconductor memory having a memory region divided into a plurality of blocks including backup blocks, the number of times data is written to each block being limited,

said method comprising the steps of:

reading data from said semiconductor memory;

performing an error-check on the read data for each block;

counting only the number of correctable errors detected by the error check of the read data, for each block and rewriting the data of a corresponding block to at least one of said backup blocks when the number of errors detected reached a preset value; and

inhibiting reuse of said block as a defective block.

13. The method according to claim 12, wherein a plurality of main blocks each having data to be subjected to an error-check, and a plurality of flash memories are used as said semiconductor memory.

## Refine Search

### Search Results -

Terms	Documents
L28 same identical	14

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L30





### Search History

DATE: Wednesday, January 28, 2004    [Printable Copy](#)    [Create Case](#)

#### Set Name Query

side by side

#### Hit Count Set Name

result set

DB=USPT; PLUR=YES; OP=OR

<u>L30</u>	l28 same identical	14	<u>L30</u>
<u>L29</u>	L28 same cell	36	<u>L29</u>
<u>L28</u>	l26 same block	196	<u>L28</u>
<u>L27</u>	L26 same sequentially	25	<u>L27</u>
<u>L26</u>	L25 same memory	537	<u>L26</u>
<u>L25</u>	ecc adj3 circuit	1035	<u>L25</u>
<u>L24</u>	l18 same block	24	<u>L24</u>
<u>L23</u>	L18 same memory	14	<u>L23</u>
<u>L22</u>	L21 same memory	4	<u>L22</u>
<u>L21</u>	l18 same l19	11	<u>L21</u>
<u>L20</u>	L19 near4 l18	6	<u>L20</u>
<u>L19</u>	circuit	961546	<u>L19</u>
<u>L18</u>	error-check	162	<u>L18</u>
<u>L17</u>	L16 same l12	3	<u>L17</u>

<u>L16</u>	correct\$ near4 writing	2322	<u>L16</u>
<u>L15</u>	L14 same l9	28	<u>L15</u>
<u>L14</u>	correct\$ same writing	10461	<u>L14</u>
<u>L13</u>	L12 and l11	24	<u>L13</u>
<u>L12</u>	l9 same writ\$	120	<u>L12</u>
<u>L11</u>	L9 same test\$	35	<u>L11</u>
<u>L10</u>	L9 same bisr	0	<u>L10</u>
<u>L9</u>	L8 same memory same cell	289	<u>L9</u>
<u>L8</u>	ecc same correct\$	5253	<u>L8</u>
<u>L7</u>	L6 same cell	18	<u>L7</u>
<u>L6</u>	L5 same memory	27	<u>L6</u>
<u>L5</u>	L4 same l3	30	<u>L5</u>
<u>L4</u>	error	376725	<u>L4</u>
<u>L3</u>	bisr	72	<u>L3</u>
<u>L2</u>	L1 same memory	40	<u>L2</u>
<u>L1</u>	ecc same repair	66	<u>L1</u>

END OF SEARCH HISTORY

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L17: Entry 3 of 3

File: USPT

Jul 19, 1983

DOCUMENT-IDENTIFIER: US 4394763 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Error-correcting system

Brief Summary Text (10):

Regarding the above mentioned 2-bit errors, the 2-bit errors may be classified into two modes or types. In a first mode or type, the 2-bit errors comprise both a first 1-bit soft error and a second 1-bit soft error both in different words. In a second mode or type, the 2-bit errors comprise both a 1-bit hard error and a 1-bit soft error. With regard to the first mode, it is easy for the ECC logic circuit to correct such 2-bit soft errors that occur in different words. This is because, as previously mentioned, the soft error does not occur repeatedly in the same memory cell. Accordingly, if the ECC logic circuit detects each soft error in one of the words and corrects the same, thereafter, the data at the corresponding memory cell can be corrected by writing the corrected data again into the same memory cell. Alternately, such soft error can also be corrected by the ECC logic circuit. That is when the ECC logic circuit detects such soft error in one of the words during an ordinary memory accessing operation, the ECC logic circuit can correct the same by rewriting the corrected data again into the same memory cell. Further, it may also be possible for the ECC logic circuit to, first scan with a certain period the memory device and read the data of all the addresses thereof sequentially, and then, if the soft error in one of the words is found, rewrite the corrected data again into the same memory cell.

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L11: Entry 34 of 35

File: USPT

Feb 16, 1988

DOCUMENT-IDENTIFIER: US 4726021 A

TITLE: Semiconductor memory having error correcting means

Detailed Description Text (30):

Checking or testing the memory after it is manufactured in accordance with this invention, includes various kinds of tests including a test for an error correcting function. In testing the semiconductor memory, it is specifically pointed out that it has a built-in error correcting function. However, if for example a single-error correcting code is used as an ECC and the memory accidentally has a defect (hard error) in one memory cell, then in this case the defect cannot be found because the readout data is corrected by the ECC, thus resulting in an apparent error-free memory.

Detailed Description Text (33):

The present invention seeks to solve this problem and provide a semiconductor memory having a built-in error correcting function using an ECC, which can test the memory cells per se for storing redundant bits of the ECC, i.e., check bits, encoding circuit, decoding circuits and the like, independently of each other.

Detailed Description Text (100):

As described, according to the present invention, in a semiconductor memory having a built-in error correcting function, writing in the memory cells for storing check bits for an ECC is performed using input data from terminal D.sub.in or data generated by an encoding circuit. On the contrary, reading data from the memory array is performed by switching between the operation and non-operation of error correction by a decoding circuit and by switching between the output and non-output of check bits. As a result, independent tests are possible, such as a test for memory cells for check bits, a test for the encoding circuit and a test for the decoding circuit.